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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
RAMPURIA, SATISH	

ART UNIT	PAPER NUMBER
2191	

DATE MAILED: 11/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/675,910	NAGARAJ ET AL.	
	Examiner	Art Unit	
	Satish S. Rampuria	2191	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/5/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the application filed on September 30, 2003.

2. Claims 1-30 are pending.

Information Disclosure Statement

3. An initialed and dated copy of Applicant's IDS form 1449 filed on July 05, 2006 is attached to the instant Office action.

Oath/Declaration

4. The Office acknowledges receipt of a properly signed oath/declaration filed February 26, 2004.

Claim Rejections - 35 USC § 101

5. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6. Claims 16-21 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claim 16 is non-statutory because the language of the claim raises a question as to whether the claim is directed merely to an abstract idea which would result in a practical application producing a concrete, useful, and tangible result to form the basis of statutory subject matter under 35 U.S.C. 101. Claim recites

compiler for developing assembly code, representing functional descriptive material without a computer readable medium or computer implemented, program (compiler) per se are not tangibly embodied. Claims 17-20 are directly or indirectly dependent on claim 16 and further compiler for developing assembly code without a computer readable medium or computer implemented, program (compiler) per se are not tangibly embodied thus amounts to only abstract idea and are nonstatutory.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1, 2, 8, 10, 17, 16, 22, 23, 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,367,071 to Cao et al. (hereinafter, Cao) in view of Published document (in May 16, 2002) by Grantson (hereinafter, Grantson).

Per claims 1, 8, and 16:

Cao disclose:

- A method, comprising: modifying source code (col. 2, lines 60-67 "...set of source code..."), including multiple instructions (col. 4, lines 34-35 "A "code block" refers generally to a set of one or more instructions"), on one or more

instructions as a function of a Digital Signal Processor (DSP) architecture (col. 3, lines 18-21 "a variety of different types of DSPs, microprocessors"); and

- generating assembly code using the modified source code (col. 2, lines 62-67 "...generates a set of code... assembly code from... source code").

Cao does not explicitly disclose by performing a Lexical Functional Grammar Analysis (LFGA) operation.

However, Grantson discloses in an analogous computer system by performing a Lexical Functional Grammar Analysis (LFGA) operation (page 1, section Introduction "...The formalism of Lexical Functional Grammar first introduced in 1982...since been applied widely to analyse...two levels of syntactic representation...c-structure...f-structure...").

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the method of using Lexical Functional Grammar Analysis as taught by Grantson into the method of Lexical Functional Grammar analysis and implementation as taught by Grantson. The modification would be obvious because of one of ordinary skill in the art would be motivated to use Lexical Functional Grammar because the Lexical Functional Grammar formalism provides a simple set of devices for describing the common properties of all human languages and the particular properties of Individual Languages as suggested by Grantson (See Abstract).

Per claims 2, 10, and 17:

The rejection of claim 1 is incorporated and further, Cao disclose:

- analyzing the modified source code for syntax and semantic (col. 5, lines 43-45 "FIG. 6 shows the assembly language syntax used to control the ZOLB in the DSP16000 processor"); and
- further modifying the source code based on the outcome of the analysis (col. 2, lines 65-67 "...applies optimization to the first set of code so as to generate a second set of code, e.g., and improved code file...").

Claims 22 and 23 are the computer product claim corresponding to method claims 1 and 2 respectively, and rejected under the same rational set forth in connection with the rejection of claims 1 and 2 respectively, above.

Claims 27, 28, and 29 are the system claim corresponding to method claims 1, 2 and 2 and rejected under the same rational set forth in connection with the rejection of claims 1, 2 and 2 respectively, above.

9. Claims 3, 18, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cao in view of Published document (in may 16, 2002) by Grantson (hereinafter, Grantson) further in view of Published document (2003) by Karttunen et al. (hereinafter, Karttunen).

Per claims 3 and 18:

The rejection of claim 2 is incorporated ad further, Cao disclose:

- changing structure of the modified source code through a series of iterations using Finite State Morphology (FSM) to generate efficient source code (col. 2, lines 65-67 "...applies optimization to the first set of code so as to generate a second set of code, e.g., and improved code file...").

Cao does not explicitly disclose using Finite State Morphology (FSM).

However, Karttunen discloses in an analogous computer system using Finite State Morphology (FSM) (page 74, section Two-level Morphology "...constructed an ingenious implementation of his constraint-based model...compiler...finite-state algorithm...called it TWO-LEVEL MORPHOLOGY...").

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the method of using Finite State Morphology (FSM) as taught by Karttunen into the method of Lexical Functional Grammar analysis and implementation as taught by the combination system of Cao and Grantson. The modification would be obvious because of one of ordinary skill in the art would be motivated to use Finite State Morphology to provide how efficient the rules could be used as suggested by Karttunen (See pages 79-80 section Reflections).

Claim 24 is the computer product claim corresponding to method claim 3, and rejected under the same rational set forth in connection with the rejection of claim 3, above.

10. Claims 4, 5, 7, 9, 11-14, 19-21, 25, 26, and 30 rejected under 35 U.S.C. 103(a) as being unpatentable over Cao in view of Published document (in may 16, 2002) by Grantson further in view of Applicant's Admitted Prior Art (hereinafter, AAPA).

Per claims 4, 11, and 19:

The rejection of claim 3 is incorporated and further, Cao disclose:

- generating intermediate code by rearranging concurrent distributed instructions based on Digital Signal Processor resources using Petri Nets algorithm (col. 2, lines 65-67 "...applies optimization to the first set of code so as to generate a second set of code, e.g., and improved code file..."); and
- generating the efficient code by selecting and comparing one or more instructions in the intermediate code to one or more other similar available instructions using Genetic algorithm (col. 2, lines 62-67 "...generates a set of code... assembly code from... source code").

Neither Cao nor Grantson explicitly discloses Petri Nets algorithm and Genetic algorithm.

However, AAPA discloses in an analogous computer system using Petri Nets algorithm and Genetic algorithm (page 5, "...Petri Nets is a mathematical tool that can be used to analyze flow of instruction in source code and to assign a flow patter...DSP

architecture") and Genetic algorithm (page 7, "...Genetic algorithms can solve complex optimization problems...").

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the method of using Petri Nets algorithm and Genetic algorithm as taught by AAPA into the method of Lexical Functional Grammar analysis and implementation as taught by the combination system of Cao and Grantson. The modification would be obvious because of one of ordinary skill in the art would be motivated to use Petri Nets algorithm and Genetic algorithm to provide a tool that yields/generates an efficient code as suggested by AAPA (See pages 5 and 8).

Per claims 5, 9, and 20:

The rejection of claim 4 is incorporated and further, Cao disclose:

- wherein the Digital Signal Processor resources are selected from the group consisting of registers, pipeline structures, instruction scheduling, memory, and MAC units (See FIG. 5 and related discussion).

Per claims 7 and 12:

The rejection of claim 4 is incorporated and further, Cao disclose:

- selecting one or more instructions from the multiple instructions that have similar available instruction sets (col. 4, lines 34-35 "A "code block" refers generally to a set of one or more instructions"); and

- performing dynamic instruction replacement on the one or more selected instructions (See FIG. 9(a)-9(c) and related discussion).

Per claim 13:

Cao disclose:

- A method of generating assembly code for execution by a DSP, comprising:
- receiving source code in higher level language including multiple instructions (col. 4, lines 34-35 "A "code block" refers generally to a set of one or more instructions");
- parsing the source code using Lexical Functional Grammar Analysis to modify one or more instructions in the program such that the modified instructions comply with specific Digital Signal Processor resources (col. 4, lines 34-35 "A "code block" refers generally to a set of one or more instructions");
- analyzing the parsed source code for syntax (col. 5, lines 43-45 "FIG. 6 shows the assembly language syntax used to control the ZOLB in the DSP16000 processor");
- updating the parsed source code for syntax based on the analysis (col. 2, lines 65-67 "...applies optimization to the first set of code so as to generate a second set of code; e.g., and improved code file...");
- generating intermediate code by rearranging concurrent distributed instructions based on the specific Digital Signal Processor resources using Petri Nets

algorithm (col. 2, lines 62-67 "...generates a set of code... assembly code from... source code");

- generating first efficient code by selecting and comparing one or more instructions in the intermediate code to one or more other similar instructions, available to process on the specific DSP, using Genetic algorithm (col. 2, lines 65-67 "...applies optimization to the first set of code so as to generate a second set of code, e.g., and improved code file...");
- selecting one or more instructions from the multiple instructions that have similar available instruction sets in the first efficient code (col. 4, lines 34-35 "A "code block" refers generally to a set of one or more instructions");
- generating second efficient code by performing dynamic instruction replacement on the one or more selected instructions(See FIG. 9(a)-9(c) and related discussion); and
- generating the assembly code by mapping the second efficient code to assembly language code (col. 2, lines 62-67 "...generates a set of code... assembly code from... source code").

Neither Cao nor Grantson explicitly discloses Petri Nets algorithm and Genetic algorithm.

However, AAPA discloses in an analogous computer system using Petri Nets algorithm and Genetic algorithm (page 5, "...Petri Nets is a mathematical tool that can be used to analyze flow of instruction in source code and to assign a flow patter...DSP

architecture") and Genetic algorithm (page 7, "...Genetic algorithms can solve complex optimization problems...").

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the method of using Petri Nets algorithm and Genetic algorithm as taught by AAPA into the method of Lexical Functional Grammar analysis and implementation as taught by the combination system of Cao and Grantson. The modification would be obvious because of one of ordinary skill in the art would be motivated to use Petri Nets algorithm and Genetic algorithm to provide a tool that yields/generates an efficient code as suggested by AAPA (See pages 5 and 8).

Per claim 14:

The rejection of claim 13 is incorporated and further, Cao disclose:

- wherein the specific Digital Signal Processor resources are selected from the group consisting of registers, pipeline structures, instruction scheduling, memory, ALUs, and MAC units (See FIG. 5 and related discussion).

Per claim 21:

The rejection of claim 20 is incorporated and further, Cao disclose:

- further comprises a database to store the Digital Signal Processor resources (See FIG. 1, element 16 and related discussion).

Claims 25 and 26 are the computer product claim corresponding to method claims 4 and 7 respectively, and rejected under the same rational set forth in connection with the rejection of claims 4 and 7 respectively, above.

Claim 30 is the system claim corresponding to method claim 4 and rejected under the same rational set forth in connection with the rejection of claim 4, above.

Allowable Subject Matter

11. Claims 6 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Satish S. Rampuria** whose telephone number is **(571) 272-3732**. The examiner can normally be reached on **8:30 am to 5:00 pm** Monday to Friday except every other Friday and federal holidays. Any inquiry of a general nature or relating to the status of this application should be directed to the **TC 2100 Group receptionist: 571-272-2100.**

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Wei Y. Zhen** can be reached on **(571) 272-3708**. The fax

phone number for the organization where this application or proceeding is assigned is **571-273-8300**.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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11.27.2006